compression/expansion circuits, the error correction processing circuits, and recording/reproduction processing circuits, and addresses of the memory are differently allotted to the respective circuits depending on the usage thereof. The superimposition data generating circuit 123 generates superimposition data by using the area 205 other than areas which are accessed by the recording/reproduction-system circuits in the memory 125. -A.

Rewrite the paragraph starting at page at page 13, line 3 and ending at page 13, line 9, as follows: --

The combining circuit 217 combines the video signal inputted from the terminal 213 and the character signal for display outputted from the table memory 211, in accordance with the operation control signal outputted from the table memory 211, and outputs the thus-obtained composite signal to an RGB conversion circuit 221 and a selector 225. A

Rewrite the paragraph starting at page at page 13, line 17 and ending at page 13, line 20, as follows:

--The RGB conversion circuit 221 converts the composite video signal outputted from the combining circuit 217 into RGB signals and outputs the RGB signals to the EVF 301.A.

Page 26, delete in its entirety and insert therefor the attached page entitled "Abstract of the Disclosure".

In the Claims

Amend claims 1, 12, 18, 20 and 29 as follows:

-- 1. (Amended) A signal processing device, comprising: